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REMARKS**INTRODUCTION:**

In accordance with the foregoing, the specification and claim 1, 2, 6, 8, 13-14, and 16-18 have been amended. Claims 3-5, 7 and 11 have been cancelled. Claim 19 has been added. Claims 1, 2, 6, 8-10, and 12-19 are pending and under consideration. No new matter is being presented.

OBJECTION FOR INFORMALITIES:

In the Office Action, at page 2, the Examiner objected to claims 1, 3, and 5 because of informalities. Claims 3 and 5 are cancelled. Applicant submits that the informality objections enumerated by the Examiner regarding claim 1, are overcome in view of the amended claim 1 as submitted herein.

PRIOR ART REJECTIONS:

In the Office Action, at pages 2-4, numbers 2-5, the Examiner rejected claims 1-9, and 13-18 as being unpatentable with regard to Ashby et al (US 6,023,196), Mole et al (US 6,060,956), and Song et al (US 6,259,321).

The reasons for the rejections are set forth in the Office Action and are therefore not repeated. The rejections are traversed, and reconsideration is requested.

Claims 3-5, and 7 have been cancelled.

THE PRESENT CLAIMED INVENTION

The current claims recite an apparatus that realizes stable high speed differential input signal switching by restraining voltage overshooting and undershooting at differential output terminals. Such undershooting and overshooting are caused by timing lags of differential input signals owing to lags in response characteristics or differences in wiring delay ensuing from hardware configuration or fluctuations in manufacturing.

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THE PRIOR ART

ASHBY

Ashby discloses "a capacitor C43 [placed] in parallel with inductor L43" (col. 3 lines 60-61) to form a "parallel resonant circuit between node 4B and the current sensing resistor R45." (col. 3 lines 57-58) The purpose of the parallel circuit is to "maximize the impedance between node 4B and ground at high frequencies" (col. 3 lines 55-56) to compensate for the fact that "at high frequencies... the operational amplifier does not have sufficient gain to force the current to be constant and common-mode performance will degrade." (col. 3 lines 52-54)

MOLE

Mole discloses transistors Q1 and Q2 that "have their emitters connected together and to constant current source K1. Capacitor C1 is connected between the emitter and collector of transistor Q1, the collector connection forming port A. Transistors Q3 and Q4 have their emitters connected together and to constant current source K2. Capacitor C2 is connected between the emitter and collector of transistor Q4, the collector connection forming port B. Port B is also connected to the collector of transistor Q2, and port A to the collector of transistor Q3; the arrangement forming a symmetrical pair of current steering circuits." (col. 5 line 62 - col. 6 line 5)

SONG

Song discloses in Fig. 1, a variable gain amplifier with an advantage that "the variable gain characteristic at high frequency is excellent...because the source connection point C of differential input transistors M51, M52 is virtual ground, and parasitic capacitance C11 of any magnitude generated in the source connection C has non influence on the variable operation. However, the variable gain amplifier of Fig 1 has the disadvantage in that case of more than hundreds of mV voltage being applied to the input, a considerable distortion is generated while the input transistor M51 or M52 departs from the conductive state. That is, the variable gain amplifier described above is not able to be used for large input." (col. 1 lines 37-48)

THE CLAIMED INVENTION PATENTABLY DISTINGUISHES OVER PRIOR ART

In contrast to the prior art, in the present invention, a capacitor is connected to a branching node for a first differential pair and a branching node for a second differential pair. The capacitor in the present invention is thereby connected between a first current source and a

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second current source in series to decrease switching noises that occur at a signal transition point of a first differential pair and a second differential pair.

Claims 1, 2 and 6 (which depend from claim 1), and 13-18 recite a structure in which a capacitor is arranged between a first branching node and a second branching node to connect the first and second current sources.

For example, claim 1 recites "a capacitor connected between the first branching node and the second branching node so that the capacitor, the first current source, and the second current source are connected ..."

Claim 13 recites "a capacitor connected between a first branching node and a second branching node for the first and second connection wiring lines from the first current source and the second current source ..."

Claim 14 recites "a capacitor connected between a first branching node and a second branching node for the first and second connection wiring from the first current source and the second current source..."

Claim 15 recites "a capacitor connected between a first branching node for branching connection wiring from the first current source to the transistors of the first conductivity type and a second branching node for branching connection wiring from the second current source to the transistors of the second conductivity type and arranged in an area surrounded by the first differential pair and the second differential pair."

Claim 16 recites "a capacitor connected between a first connection node between the first differential input unit and the first current supply unit and a second connection node between the second differential input unit and the second current supply unit so that the capacitor, the first current supply unit, and the second current supply unit are connected..."

Claim 17 recites "a capacitor connected between a first connection node and a second connection node, the first and second connection nodes respectively connecting the first current supply unit to the first differential input unit and the second current supply unit to the second differential input unit..."

And claim 18 recites "a capacitor connected between a connection node between the first differential input unit and the first current supply unit, and another connection node between the second differential input unit and the second current supply unit."

Similarly, claim 8 recites "a first current source, connected to one end of the first

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differential pair at a first branching node branching current from the first current source to the first transistors; a second differential pair receiving the differential signals, said second differential pair having second transistors; a second current source connected to one end of the second differential pair at a second branching node branching current from the second current source to the second transistors; and a transitional response circuit forming a current path allowing one of the current supplied from one of the first and second current sources to flow when the current to one of the first and second differential pair is cut off."

And claim 9 recites "The differential signal output apparatus, as claimed in Claim 8, wherein: the transitional response circuit is a capacitor."

Ashby, Mole, and Song do not disclose a structure with a capacitor connected to a branching node for a first differential pair and a branching node for a second differential pair.

The structure recited in the current claims realizes stable high speed differential input signal switching by restraining voltage overshooting and undershooting at differential output terminals, thereby decreasing switching noises that occur at a signal transitional point of a first differential pair and a second differential pair.

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CONCLUSION:

Accordingly, applicant asserts that claims 1, 2, 6, 8-10, and 12-18 are patentably distinguishable over the cited prior art, and should be allowable for at least the above-mentioned reasons.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8(a)
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on June 25 2003
for STAAS & HALSEY
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Please Note Effective June 28, 2003, Staas & Halsey LLP will be moving to the following address:

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